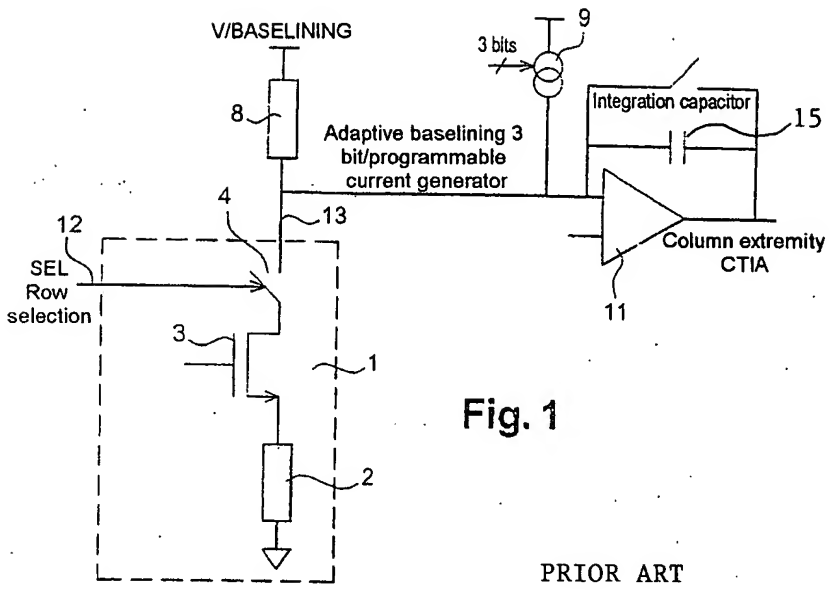


Fig. 1

PRIOR ART

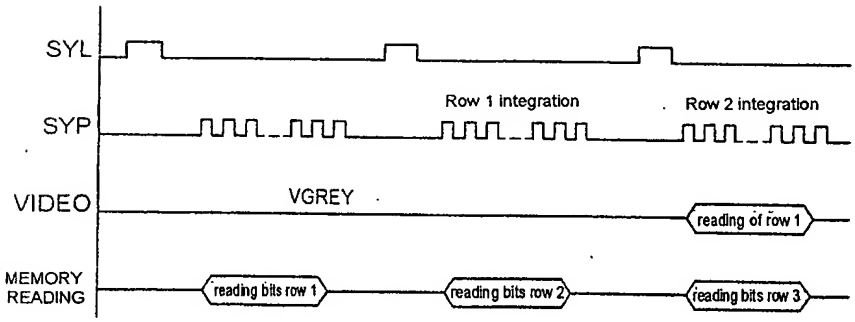


Fig. 2

PRIOR ART

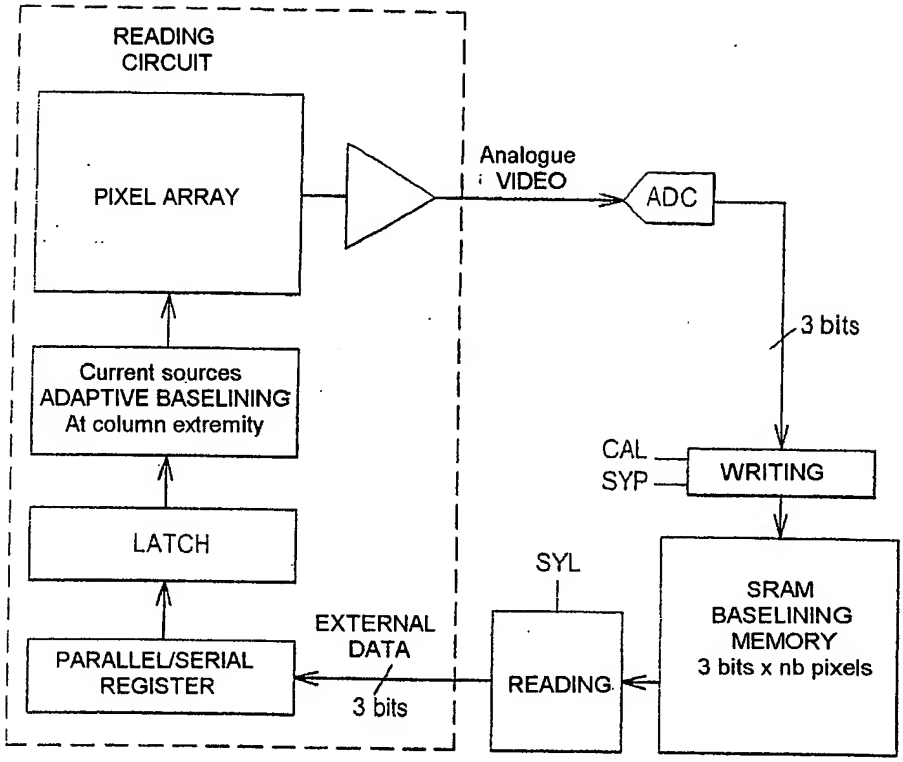


Fig. 3

PRIOR ART

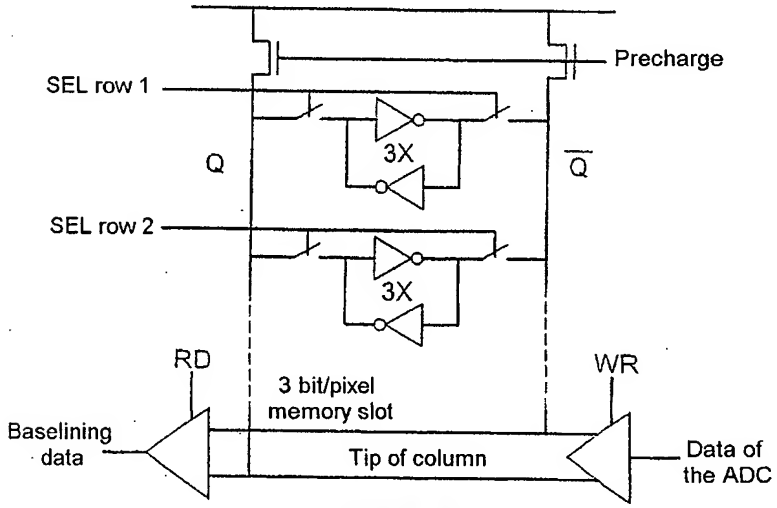
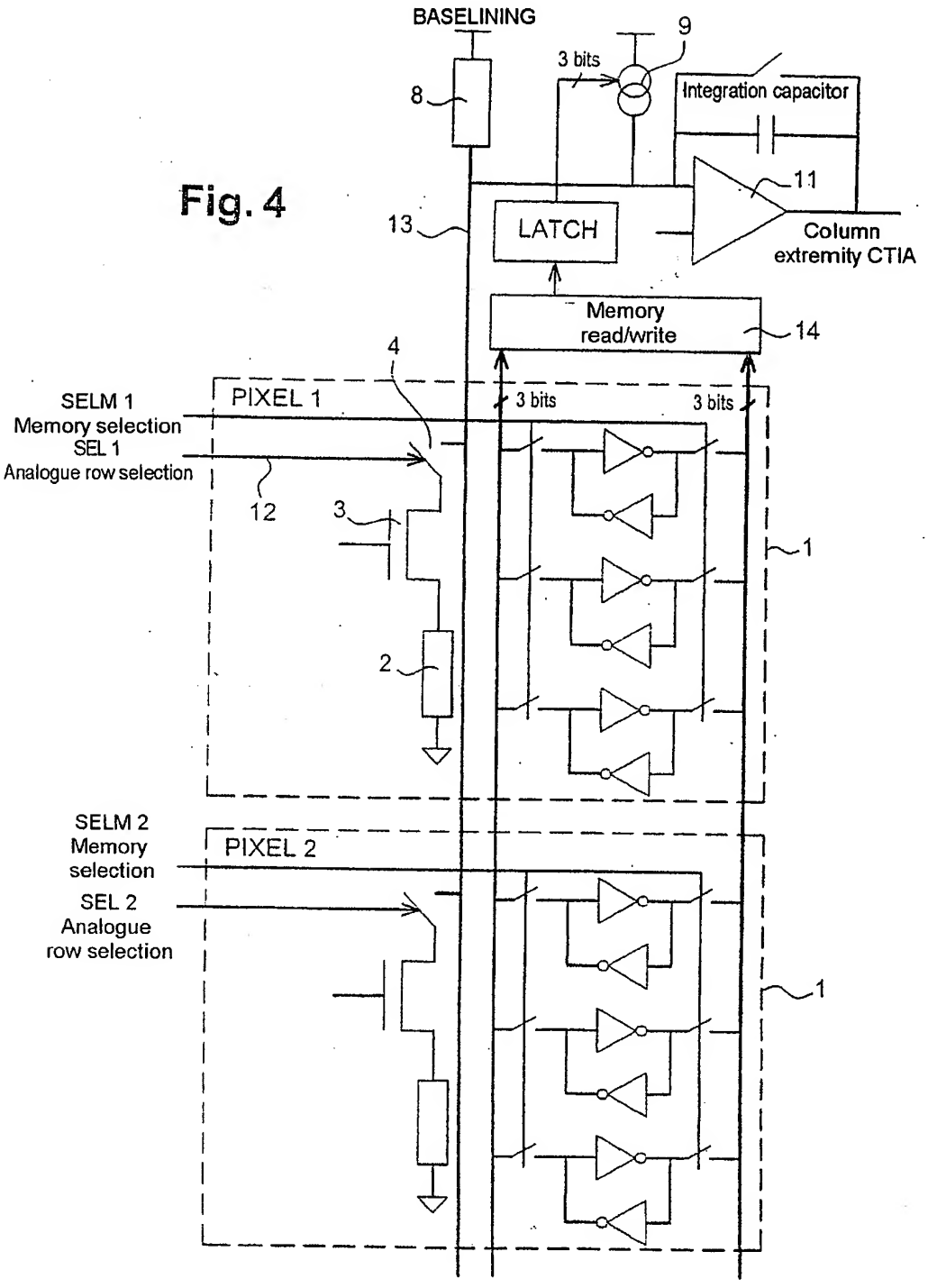


Fig. 5

Fig. 4


BASELINING
9
3 bits
8
Integration capacitor
11
13
LATCH
Column extremity CTIA
Memory read/write
14
4
SELM 1
Memory selection
SEL 1
Analogue row selection
PIXEL 1
3 bits
3 bits
12
3
1
2
SELM 2
Memory selection
SEL 2
Analogue row selection
PIXEL 2
1